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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,324	05/18/2005	Mark J. Childs	GB020201US	5728

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CHOW, YUK	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
03/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,324	CHILDS, MARK J.	
	Examiner	Art Unit	
	YUK CHOW	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/17/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/17/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
It does not state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56.

OATH OR DECLARATION
§ 1.63 Oath or declaration.
(a) An oath or declaration filed under § 1.51(b)(2) as a part of a nonprovisional application must:
(1) Be executed, i.e., signed, in accordance with either § 1.66 or § 1.68. There is no minimum age for a person to be qualified to sign, but the person must be competent to sign, i.e., understand the document that the person is signing;
(2) Identify each inventor by full name, including the family name, and at least one given name without abbreviation together with any other given name or initial;
(3) Identify the country of citizenship of each inventor; and
(4) State that the person making the oath or declaration believes the named inventor or inventors to be the original and first inventor or inventors of the subject matter which is claimed and for which a patent is sought.
(b) In addition to meeting the requirements of paragraph (a) of this section, the oath or declaration must also:
(1) Identify the application to which it is directed;
(2) State that the person making the oath or declaration has reviewed and understands the contents of the application, including the claims, as amended by any amendment specifically referred to in the oath or declaration; and
(3) **State that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56.**
(c) Unless such information is supplied on an application data sheet in accordance with § 1.76, the oath or declaration must also identify:

The oath or declaration needs to be consistent with MPEP according to the Office's policy, correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 4 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ochi et al. (US 2003/0107537).

As to claim 1, Ochi discloses a colour active matrix electroluminescent display device comprising a row and column array of display pixels [1], each pixel comprising

an electroluminescent display element [2] (Fig. 1(1R)) and

a drive transistor [22] for driving a current through the display element (Fig. 7(11R)),

the drive transistor and the display element being connected in series between a power line [26] for supplying or drawing a controllable current to or from the display element and a common potential line [30] (see [0022] and Fig. 7),

wherein each row of display pixels comprises different colour display pixels for producing different colour light outputs (See Fig. 7(RGB)),

wherein the display pixels of each colour in a row are associated with a respective and separate power line [26', 26", 26"'] (see lines connect to Fig. 7(22R, 22G, 22B)), and

wherein the power supply to each power line is individually switchable [40, 45, 48] so as to control the duty cycle of the associated display pixels (See Fig. 7(23R, 23G, 23B)).

As to claim 2, Ochi discloses a display device according to claim 1, wherein the power lines [26', 26", 26'"] associated with the rows of pixels are connected to a power supply [40] (see Fig. 7(21)) through a switching arrangement [45] at one end of the rows.

As to claim 3, Ochi discloses a display device according to claim 2, wherein the power lines associated with a row of pixels are connected to at least one power supply rail through respective switches [36, 37, 38] (See Fig. 7(23R, 23G, 23B)) of the switching arrangement [45] (see [0022], the switches are turned on by a control circuit).

As to claim 4, Ochi discloses a display device according to claim 3, wherein the number of power supply rails corresponds to the number of power lines associated with a row of pixels and the power supply rails are shared by all the rows of pixels (see Fig. 7, three power lines connect to three power supply rails (22R, 22G, 22B) and all shared by all rows of pixels).

As to claim 10, Ochi discloses a display device according to claims 2 wherein the switching arrangement is fabricated on a substrate of the device carrying the display pixels and power lines (see Fig. 4 and 5, although Ochi does not explicitly state that switching arrangement is fabricated on a substrate, it is a well known in the art to fabricate switching arrangement on a substrate, also it is inherent to place functionally

related components near-by or in a group, so that simplified routing improves switching speed and keep the cost of the fabrication down).

As to claim 11, Ochi discloses a display device according to claim 1, wherein each row of display pixels comprises red, green, and blue pixels, the different colour pixels being connected to respective power lines (see Fig. 7, three power lines connect to three power supply rails (22R, 22G, 22B)).

As to claim 12, Ochi discloses a display device according to claim 1, wherein the power supply to the power lines for the display pixels of same colour in different rows are individually switchable so as to separately control the duty cycle of each row of display pixels of the same colour (see Fig. 7(24i, 24i+1) in conjunction with 23R, 23G, 23B to turn on/off the each row of display pixels, see [0022]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi in view of Nakamura (US 2003/0043132).

As to claim 5, Ochi discloses a display device according to claim 3 above.

However, Ochi does not explicitly teach each frame period [T_f] each row of pixels is arranged to be addressed in sequence in a respective row address period [T_r] so as

to store a drive signal for controlling the operation of the drive transistor [22] of the pixels.

Nakamura discloses a display device wherein teaches control signals consists of frame period (Fig. 3(T2)) is to be addresses in sequence in a respective row address period (Fig. 3(scanning signal (n, n+1…)), also to store a drive signal in a latch circuit (see Fig. 2(24B)).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to use sequential distribution of signal as in Nakamura into display device of Ochi, due to the fact that sequential driving technique are common and simple to control (see Nakamura [0009]-[0010]).

As to claim 6, Ochi and Nakamura disclose a display device according to claim 5, wherein the switching arrangement [45] is operable to connect each of the power lines associated with a row of pixels to the power supply [40] for a predetermined period following addressing which determines the duty cycle of the display pixels associated with the power line, the power lines of each row of pixels being switched in similar manner in sequence (see Nakamura Fig. 3(ASW1, ASW2, ASW3) and [0044]).

As to claim 7, Ochi and Nakamura disclose a display device according to claim 6, wherein the power lines of a row are connected to the power supply [40] for a predetermined period that immediately follows the row address period [T_r] (see Nakamura Fig. 3(ASW1, ASW2, ASW3) for a predetermined period follows the row address (n-th) scanning line).

As to claim 8, Ochi and Nakamura disclose a display device according to claims 5, wherein each pixel includes a storage capacitor [24] (see Nakamura Fig. 1(18)) for storing a gate voltage of the drive transistor [22] (Fig. 1(17)) and an address transistor [16] (Fig. 1(13)) for switching a data voltage to the gate of the drive transistor during the row address period, and wherein the switching arrangement [45] is operable to disconnect the power lines of a row of pixels from the power supply during the row address period (see Fig. 2 and [0039]).

As to claim 9, Ochi and Nakamura disclose a display device according to claims 5, wherein the pixels each include a current sampling circuit for sampling a drive current during the row address period and a storage capacitor for storing a gate--source voltage for the drive transistor corresponding to the sampled drive circuit and wherein the switching arrangement is operable to connect the power lines associated with a row of pixels to the power supply during the row address period (It's well known that pixel circuit using additional circuit for monitoring or ageing compensation, since this is a current-addressed type pixel display circuit, see Nakamura [0035]-[0038], it's inherent to include a current sampling circuit).

Response to Arguments

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUK CHOW whose telephone number is (571)270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. C./
Examiner, Art Unit 2629
03/17/2008

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629